



Attorney Docket No. 50275-0014  
5GAU 2812

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

MAR 26 2001  
In re application of:  
TECHNOLOGY CENTER 2800  
Christophe Pierrat, et al.

Group Art Unit No.: 2812

Examiner: NYA

Serial No.: 09/675,197

Filed on: September 29, 2000

For: DISSECTION OF EDGES WITH PROJECTION  
POINTS IN A FABRICATION LAYOUT FOR  
CORRECTING PROXIMITY EFFECTS —

Commissioner for Patents  
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

This Information Disclosure Statement is being submitted under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The Examiner's attention is directed to the following co-pending U.S. Patent Applications:

U.S. patent application serial number 09/130,996, entitled "Visual Inspection and Verification System," filed on August 7, 1998;

U.S. patent application serial number 09/153,783, entitled "Design Rule Checking System and Method," filed on September 16, 1998;

U.S. patent application serial 09/544,798, entitled "Method and Apparatus for a Network Based Mask Defect Printability Analysis System," filed on April 7, 2000;

U.S. patent application serial number 09/154,415, entitled "Data Hierarchy Layout Correction and Verification Method and Apparatus," filed on September 16, 1998;

U.S. patent application serial number 09/154,397, entitled "Method and Apparatus for Data Hierarchy Maintenance in a System for Mask Description," filed on September 16, 1998; and

U.S. patent application serial number 09/632,080, entitled "General Purpose Shape-Based Layout Processing Scheme for IC Layout Modifications," filed on August 2, 2000,

which are directed to related technical subject matter. The identification of these U.S. Patent Applications is not to be construed as a waiver of secrecy as to these applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.



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Throughout the pendency of this application, please charge any additional fees, including  
any required extension of time fees, and credit all overpayments to deposit account 50-1302. A  
duplicate of this sheet is enclosed.

Respectfully submitted,

HICKMAN PALERMO TRUONG & BECKER LLP

Dated: March 16, 2001

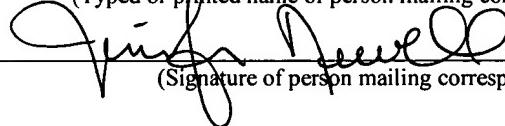
  
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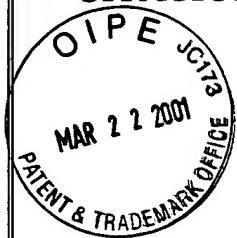
Jennifer Newell

(Typed or printed name of person mailing correspondence)

  
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(Signature of person mailing correspondence)

<b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  <b>(PTO-1449)</b>			ATTY. DOCKET NO. <b>50275-0014</b>	SERIAL NO., <b>09/675,197</b>			
			APPLICANT <b>Christophe Pierrat, et al.</b>				
			FILING DATE <b>September 29, 2000</b>	GROUP <b>2812</b>			
<b>U.S. PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
	4,812,962	03/14/89	Witt				
	5,051,598	09/24/91	Ashton, et al.				
	5,182,718	01/26/93	Harafugi, et al.				
	5,241,185	08/31/93	Meiri, et al.				
	5,242,770	09/07/93	Chen, et al.				
	5,256,505	10/26/93	Chen, et al.				
	5,316,878	05/31/94	Saito, et al.				
	5,326,659	07/05/94	Liu, et al.				
<b>FOREIGN PATENT DOCUMENTS</b>						Translation	
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Yes	No
	WO 00/67074	11/09/00	PCT				
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)</b>							
	Barouch, E., et al., "OPTIMASK: An OPC Algorithm for Chrome and Phase-Shift Mask Design", 2/22-24/95, SPIE Vol. 2440, pp. 192-206.						
	Brunner, T., et al., "Approximate Models for Resist Processing Effects", 198/SPIE Vol. 2726, Optical Microlithography IX, 13-15 March 1996, pp. 198-209.						
	Brunner, T., "Rim Phase-Shift Mask Combined with Off-Axis Illumination: A Path to 0.5λ/Numerical Aperture Geometries", Optical Engineering, October 1993, Vol. 32 No. 10, pp. 2337-2343.						
	Casey, J. Jr., et al., "Chemically Enhanced FIB Repair of Opaque Defects on Molybdenum Silicide Photomasks", Wednesday Poster Session Paper 3236-58, Photomask Technology and Management Technical Program, (1997), SPIE Vol. 3236, pp. 487-497.						
	Chang, K., et al., "Accurate Modeling of Deep Submicron Interconnect Technology", TMA Times, Fall 1997 Volume IX, No. 3.						
	Cobb, et al., "Fast Sparse Aerial Image Calculation for OPC", SPIE Vol. 2621, pp. 534-544.						
	Gans, F., et al., "Printability and Repair Techniques for DUV Photomasks", Photomask Technology and Management Technical Program, Session 3 Paper, (1998), pp. 136-141.						
	Ham, Y. M., et al., "Dependence of Defects in Optical Lithography", Jpn. J. Appl. Phys. Vol. 31 (1992), pp. 4137-4142.						
EXAMINER			DATE CONSIDERED				

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

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EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,340,700	08/23/94	Chen, et al.			
	5,424,154	06/13/95	Borodovsky			
	5,432,714	07/11/95	Chung, et al.			
	5,447,810	09/05/95	Chen, et al.			
	5,533,148	06/02/96	Sayah, et al.			
	5,538,815	07/23/96	Oi, et al.			
	5,553,273	09/03/96	Liebmann			
	5,572,598	11/05/96	Wihl, et al.			
<b>FOREIGN PATENT DOCUMENTS</b>						
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation
						Yes
	WO 00/67075	11/09/00	PCT			
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)</b>						
	Henke, W., et al., "A Study of Reticle Defects Imaged Into Three-Dimensional Developed Profiles of Positive Photresist Using the SOLID Lithography Simulator", Microelectronic Engineering 14 (1991) 283-297.					
	Ibsen, K., et al., "Clear Field Reticle Defect Disposition for Advanced Sub-Half Micron Lithography", (1997), Photomask Technology and Management Technical Program, Session 3 Paper 3236-13.					
	Ishiwata, N., et al., "Novel Alternating Phase Shift Mask with Improved Phase Accuracy", Photomask Technology and Management Technical Program, Session 7 Paper 3236-28, SPIE Vol. 3236.					
	Jinbo, H., et al., "0.2μm OR Less i-Line Lithography by Phase-Shifting-Mask Technology", Semiconductor Technology Lab., Oki Electric Industry Co., Ltd., CH2865-4/90/0000-0825, pp. 33.3.1-33.3.4.					
	Jinbo, H., et al., "Application of Blind Method to Phase-Shifting Lithography", 1992 Symposium on VLSI Technology Digest of Technical Papers, pp. 112-113.					
	Jinbo, H., "Improvement of Phase-Shifter Edge Line Mask Method", Japanese Journal of Applied Physics, Vol. 30, No. 11B, November, 1991, pp. 2998-3003.					
	Karklin, Linard, "A Comprehensive Simulation Study of the Photomask Defects Printability", SPIE Vol. 2621, pp. 490-504.					
	Kimura, T., et al., "Subhalf-Micron Gate GaAs Mesfet Process Using Phase-Shifting-Mask Technology", GaAs IC Symposium, 1991, pp. 281-284.					
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	5,631,110	05/20/97	Shioiri, et al.			
	5,657,235	08/12/97	Liebmann, et al.			
	5,663,893	09/02/97	Wampler, et al.			
	5,702,848	12/30/97	Spence			
	5,705,301	01/06/98	Garza, et al.			
	5,707,765	01/13/98	Chen			
	5,740,068	04/14/98	Liebmann, et al.			
	5,795,688	08/18/98	Burdorf, et al.			

**FOREIGN PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No
	WO 00/67076	11/09/00	PCT				

**OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

Lithas: Optical Proximity Correction Software
MicroUnity: OPC Technology & Product Description, pp. 1-5.
Morimoto, H., et al., "Next Generation Mask Strategy-Techologies are Ready for Mass Production of 256MDRAM?", (Panel discussion of PMJ'97 on Apr. 18, 1997), SPIE Vol. 3236 pp. 188-189.
Nistler, J., et al., "Large Area Optical Design Rule Checker for Logic PSM Application", SPIE Vol. 2254 Photomask and X-Ray Mask Technology (1994), pp. 78-92.
Nistler, J., et al., "Phase Shift Mask Defect Printability Analysis", Eytan Barouch and Uwe Hollerbach, Princeton University, Princeton, NJ, pp. 11-27.
Ohtsuka, H., et al., "Phase Defect Repair Method for Alternating Phase Shift Masks Conjugate Twin-Shifter Method", Jpn. J. Appl. Phys. Vol 31, Part 1, No. 12B, (1992) pp. 4143-4149.
Park, C., et al., "An Automatic Gate CD Control for a Full Chip Scale SRAM Device", CAE, Process Development Team, Semiconductor R&D Center, Samsung Electronics Co, Ltd, SPIE Vol. 3236, (1997), pp. 350-356.
Pati, Y.C., et al., "Exploiting Structure in Fast Aerial Image Computation for Integrated Circuit Patterns", IEEE Transactions on Semiconductor Manufacturing, Vol. 10. No. 1, February 1997, pp. 62-74.
Pati, Y.C., et al., "Phase-Shifting Masks for Microlithography: Automated Design and Mask Requirements," J. Opt. Soc. Am. A/Vol. 11, No. 9/September 1994, pp. 2438-2452.
"Proxima System," Precim Company, Portland, Oregon (2 pages).

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	5,801,954	09/01/98	Le, et al.				
	5,804,340	09/08/98	Garza, et al.				
	5,815,685	09/29/98	Kamon				
	5,825,647	10/20/98	Tsudaka				
	5,827,623	10/27/98	Ishida, et al.				
	5,847,959	12/08/98	Veneklasen, et al.				
	5,849,440	12/15/98	Lucas, et al.				
	5,863,682	01/26/99	Abe, et al.				
	6,081,658	06/27/00	Rieger, et al.				
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<ul style="list-style-type: none"> <li>· "Proxima Wafer Proximity Correction System", Precim Company, Portland, Oregon (2 pages).</li> <li>· Rieger, M., et al., "Customizing Proximity Correction for Process-Specific Objectives", Precim Company, (1996), SPIE Vol. 2726, pp. 651-659.</li> <li>· Rieger, M., et al., "Mask Fabrication Rules for Proximity-Corrected Patterns", Precim Company, Portland, Oregon.</li> <li>· Rieger, M., et al., "Proxima System Theory of Operation", August 23, 1993, pp. 1-20.</li> <li>· Rieger, M., et al., "V-Domain Definition", September 8, 1993, pp. 1-7.</li> <li>· Rieger, M., et al., "Using Behavior Modelling for Proximity Correction", Precim Company, SPIE 1994.</li> <li>· Roman, B., et al., "Implications of Device Processing on Photomask CD Requirements", (Motorola Advanced Products Research and Development Laboratory, Austin, TX 78762), Photomask Technology and Management Technical Program, Session 8, Paper 3236-31, page 51.</li> <li>· Spence, C., et al., "Automated Determination of CAD Layout Failures Through Focus: Experiment and Simulation", SPIE Vol. 2197, (1994), pp. 302-313</li> <li>· Spence, C., et al., "Detection of 60° Phase Defects on Alternating PSMs", Advanced Micro Devices, KLA-Tencor DuPoint TRC.</li> <li>· Stirnimann, J., et al., "Fast Proximity Correction with Zone Sampling", SPIE Vol. 2197 (1994), pp. 294-301.</li> </ul>							
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<ul style="list-style-type: none"> <li>- Stirniman, J., et al., "Optimizing Proximity Correction for Wafer Fabrication Processes", SPIE Vol. 2322, Photomask Technology and Management (1994), pp. 239-246.</li> <li>- Stirniman, J., et al., "Spatial Filter Models to Describe IC Lithographic Behavior", Precim Corporation, Portland, Oregon.</li> <li>- Stirniman, J., et al., "Wafer Proximity Correction and Its Impact on Mask-Making", Bacus News, Photomask, January 1994, Volume 10, Issue 1, p. 1, 3-7, 10-12.</li> <li>- Sugawara, M., et al., "Defect Printability Study of Attenuated Phase-Shifting Masks for Specifying Inspection Sensititvity", Semiconductor Company, Sony Corporation, Kanagawa, Japan.</li> <li>- Trans Vector Technologies, Inc: "Now Better Quality Photomasks", OPRX, 4 pages.</li> <li>- Vacca, A., et al., "100nm Defect Detection Using a Dynamically Programmable Image Processing Algorithm", Photomask Technology and Management Technical Program, Session 6 Paper 3236-24.</li> <li>- Vacca, A., et al., "100nm Defect Detection Using an Existing Image Acquisition System", (1998), SPIE Vol. 3236, pp. 208-214.</li> <li>- Watanabe, H., et al., "Detection and Printability of Shifter Defects in Phase-Shifting Masks II. Defocus Characteristics", Jpn. J. Appl. Phys. Vol. 31 (1992) Pt. 1, No. 12B, pp. 4155-4160.</li> <li>- Wiley, J., et al., "Device Yield and Reliability by Specification of Mask Defects", SolidState Technology, Lithography.</li> <li>- Wiley, J., et al., "The Effect of Off-Axis Illumination on the Printability of Opaque and Transparent Reticle Defects", SPIE Vol. 2512, (1995), pp. 432-440.</li> <li>- Wiley, J., et al., "Phase Shift Mask Pattern Accuracy Requirements and Inspection Technology", SPIE Vol. 1464 Integrated Circuit Metrology, Inspection and Process Control V (1991), pp. 346-355.</li> <li>- Yen, A., et al., "Characterization and Correction of Optical Proximity Effects in Deep-Ultraviolet Lithography Using Behavior Modeling", J. Vac. Sci. Technol. B 14(6), Nov/Dec 1996, pp. 4175- 4178.</li> </ul>							
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